N.A.T. Eth29-G

Technical Reference Manual V1.5

Hardware Revision 1.1

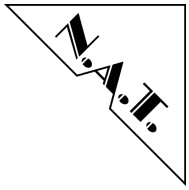

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Table of Contents

1 BOARD SPECIFICATION 7

2 STATEMENT ON ENVIRONMENTAL PROTECTION 8

2.1 COMPLIANCE TO ROHS DIRECTIVE 8
2.2 COMPLIANCE TO WEEE DIRECTIVE 8
2.3 COMPLIANCE TO CE DIRECTIVE 9

3 INTRODUCTION 10

3.1 TECHNICAL SPECIFICATIONS 11

4 HARDWARE DESCRIPTION 13

4.1 ETH29-G – LOCATION OVERVIEW 13
4.2 VMEBUS INTERFACE 14
4.3 PROCESSOR BLOCK – FREESCALE POWERQUICC II PRO 14
4.4 NETWORK INTERFACE 14
4.5 DUAL-PORTED RAM 15
4.6 REAL TIME CLOCK SUPPORT 15
4.7 SERIAL LINE INTERFACES 15
4.8 USB INTERFACES 15

5 ETH29-G - JUMPER SETTINGS 16

5.1 SETTING THE BOARD´S BASE ADDRESS 16
5.2 SETTING THE VMEBUS INTERRUPT VECTOR/LEVEL 16
5.3 BDM TEST CONNECTOR 16

6 THE ETH29-G FRONT-PANEL 18

6.1 RESET SWITCH 19
6.2 BOARD STATUS INDICATOR LEDS 19
6.3 NETWORK INDICATOR LEDS 19
6.4 RS232 INTERFACES - S1 AND S2 20
6.5 USB CONNECTORS 20
6.6 10/100/1000 BASET CONNECTORS 21

7 ADDRESS RANGES 22

7.1 VMEBUS – ADDRESSES 22
7.2 POWERQUICC II PRO CPU - MEMORY MAP 23
7.3 POWERQUICC II PRO CPU - IRQ MAP 23

8 REGISTERS 24

8.1 ACCESSING MAILBOX AND SOFTWARE-RESET LOCATIONS 24
8.2 FPGA INTERNAL REGISTERS 25
8.2.1 FPGA Version Register 25
8.3 CPLD INTERNAL REGISTERS 25
8.3.1 PCB Version Register 25
8.3.2 CPLD Version Register 25
8.3.3 CPLD Status/Control Register 1 26
8.3.4 CPLD Status/Control Register 2 26
8.3.5 CPLD Status/Control Register 3 27

9 BUS INTERRUPTER MODULE 28

10 KNOWN BUGS 29

APPENDIX A: REFERENCE DOCUMENTATION 30

APPENDIX B: DOCUMENT'S HISTORY 31

List of Tables

TABLE 1:	NAT-ETH29-G FEATURES	7
TABLE 2:	BDM TEST CONNECTOR	16
TABLE 3:	PROGRAMMABLE GP LEDS	19
TABLE 4:	PROGRAMMABLE NETWORK LEDS	19
TABLE 5:	RS232 CONNECTORS	20
TABLE 6:	USB CONNECTORS	20
TABLE 7:	10/100/1000 BASET CONNECTORS	21
TABLE 8:	VMEBUS – ADDRESSES	22
TABLE 9:	POWERQUICC II PRO CPU - MEMORY MAP	23
TABLE 10:	POWERQUICC II PRO CPU - IRQ MAP	23
TABLE 11:	FPGA VERSION REGISTER	25
TABLE 12:	PCB VERSION REGISTER	25
TABLE 13:	CPLD VERSION REGISTER	25
TABLE 14:	CPLD STATUS/CONTROL REGISTER 1	26
TABLE 15:	CPLD STATUS/CONTROL REGISTER 1	26
TABLE 16:	CPLD STATUS/CONTROL REGISTER 1	27

List of Figures

FIGURE 1:	ETH29-G – LOCATION OVERVIEW	13
FIGURE 2:	THE ETH29-G FRONT-PANEL	18

1 Board Specification

Table 1: NAT-ETH29-G Features

Power Consumption	5V / 1.7A max. *(Without current draw on USB Connector power Pins)*	
Environmental Conditions	Temperature (operating):	0°C to +50°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
MTBF calculation	5.10 years at 25°C (MIL217F)	
Standards Compliance	ANSI/VITA VMEBUS Specification	
Product Safety	The board complies with EN60950 and UL1950	

2 Statement on Environmental Protection

2.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

3 Introduction

The Eth29-G is an intelligent high performance VMEbus Ethernet controller board. It has been designed to support high data transfer rates with a minimum of impact on the system load of the host system.

The board combines a true 32-bit architecture with a powerful RISC processor to enable the utilization of the Ethernet network´s maximum throughput. A Freescale PowerQUICC II Pro processor handles all of the local network protocols up to layer 4 and thus enables an effective transfer rate of up to 30 MByte/sec with all network protocols.

The Eth29-G board supports all of today´s standard protocols (TCP/IP, DECNet, ISO/OSI protocol) and is prepared for tomorrow´s demands. All of the N.A.T. network protocols are based on N.A.T.´s Universal Protocol Stack Architecture (UPSA) which supports the simultaneous and independent execution of different network protocols on the Eth29-G board.

The Eth29-G handles the processor-intensive network protocols onboard. Thus, the system´s main processor is free and the real-time capability of the system is undiminished by even high network traffic. The board´s VMEbus interface achieves short bus cycles through the use of intelligent access modes. Thus, high network data transfer rates are also achieved with standard (D16) CPU boards that provide no support for Block-Transfer or DMA.

The Eth29-G board is delivered with the multi-tasking kernel OK1 (Open Kernel 1). OK1 supplies all of the operating system resources required by the network software. For a detailed description of the OK1 kernel please refer to the "N.A.T. OK1 Reference Manual".

3.1 Technical Specifications

Bus Interface:
- VMEbus Rev. C1, ANSI/IEEE STD1014-1987
- D32/A32, D16/A24
- all standard and extended addressing modes
- Block mode data transfers
- VMEbus interrupter and Mailbox IRQs
- Auto Slot ID cycle support

Processor:
- Motorola PowerQUICC II Pro

CPU-Type	Speed	
MPC8347(E)VRALF	667 MHz	optional
MPC8347(E)VRAGD	400 MHz	optional
MPC8343(E)VRAGD	400 MHz	assembled (standard)

- e300 Core
- 32 KByte Data- and 32 KByte Instruction Cache
- Floating Point Unit
- Security Engine (E-Versions)
- 4-channel DMA controller
- DRAM Controller, supports DDR SDRAM
- Local Bus controller, supports SRAM, SDRAM, EDO and page mode DRAM
- 2 Universal Synchronous/Asynchronous Receiver/Transmitters (UART)
- 8 16-Bit General-Purpose Multimode Timers
- Dual 3-speed Ethernet Controller (10/100/1000)
- Dual USB 2.0 multi-port host controller
- Dual I^2C®-Compatible Bus
- 32 bit PCI Interface, host and agent mode
- programmable Interrupt controller
- System Debug Support
- Clock Multiplied PLL
- up to 64 general-purpose parallel I/O ports

Memory:
- Communication RAM: 4 MB dual ported RAM
- Processor RAM: 64 MB DDR SDRAM (optional up to 256 MB)
- 16 MB Flash EEPROM for onboard firmware, 512 KB Fallback FLASH

Network:
- RGMII dual 3-speed Ethernet PHY Broadcom BCM5482
- 10/100/1000 Mbit twisted pair interface 10BaseT, 100BaseT, 1000BaseT

I/O:
- 2 serial Line Interfaces RS232
- 2 USB 2.0 multi-port host/agent Interfaces

Protocols:
- TCP/IP
- DECNet
- ISO/OSI
- OS-9 Net
- simultaneous handling of different protocols onboard

Host Driver Support:
- OS9
- VxWorks

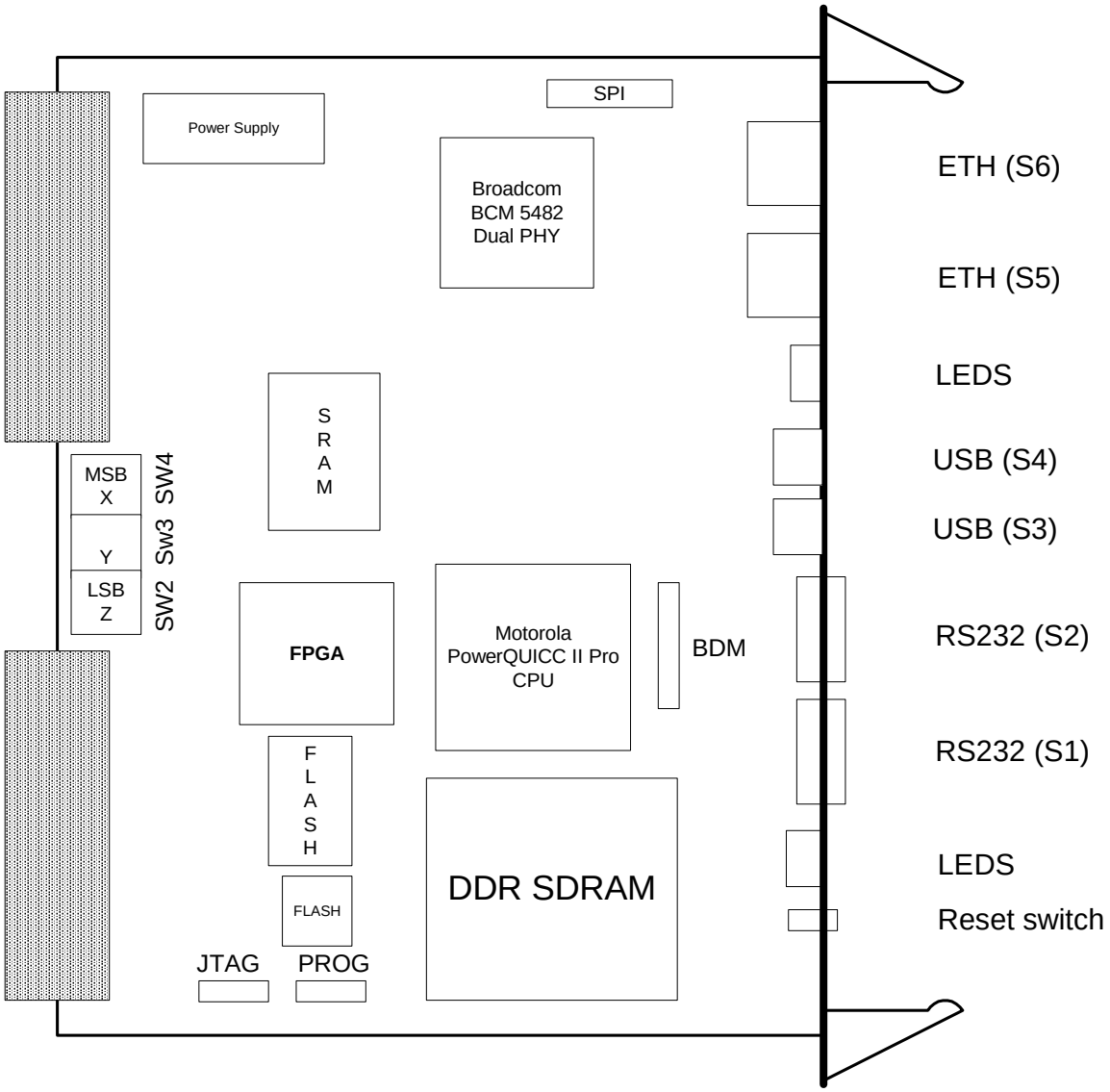
Throughput:
- tbd

4 Hardware Description

This chapter contains a brief description of the functional blocks of the Eth29-G board.

4.1 Eth29-G – Location Overview

Figure 1: Eth29-G – Location Overview



4.2 VMEbus Interface

The VMEbus interface on the Eth29-G Ethernet board meets the VMEbus standard Rev. C.1 (ANSI/IEEE STD1014-1987). In the basic configuration, the Eth29-G is a slave board. The board can be operated in either D32/A32 or D16/A24 modes. It supports all standard and extended address modes. It always occupies a 4 MByte address range on the VMEbus (factory setting), which also includes cells for mailbox interrupts and a software reset (see chapter 7). The board can trigger a level 1 - 7 VMEbus vector interrupt.
Additionally the new generation Eth29-G Boards will support the Auto Slot ID cycle according to the VME64 specification. This includes an area of memory where configuration and version informations are stored (even if the auto Slot ID mechanism is not used). This memory area is accessible from the VMEbus side.

4.3 Processor Block – Freescale PowerQUICC II Pro

The Freescale PowerQUICC II Pro ®, MPC8343/MPC8347, are high performance, low-cost, highly integrated microprocessors, designed for embedded control applications, which combine an e300 processor core with two Multiply Accumulate (MAC) units, 32- or 64-bit DDR SDRAM controller, DMA controller, timers, and parallel and serial interfaces. The PowerQUICC II Pro ® packaging provides common system functions on chip, and glueless interfaces to 8-, 16-, and 32-bit (S)DRAM, SRAM, ROM, and I/O devices.
For further information please refer to the devices User's Manual, listed under Appendix A at the end of this document.

4.4 Network Interface

The Eth29-G board comes with an interface to connect 2 RJ45 connectors for 10/100/1000BaseT interfaces. All network connectors are located on the board´s front-panel.
The dual 3-speed Broadcom BCM5482, which has a RGMII interface, is used as the Ethernet PHY. The processor can communicate with the integrated Ethernet Controller as a slave device or by DMA transfer, with the network packets being written to and read from the multiport RAM.
For further information please refer to the devices User's Manual, listed under Appendix A at the end of this document.

4.5 Dual-ported RAM

Communication between the VMEbus interface, onboard processor and integrated network controller is done via a fast dualported RAM which can be accessed simultaneously from all ports. The multiport RAM is equipped with 4 MByte of SRAM. All N.A.T. network protocols are written to use the minimum number of copy operations; thus, user data that is written by the master CPU board into the dualport RAM can be transferred by the integrated Ethernet controller using DMA transfers directly into the network.
For further information please refer to the devices User's Manual, listed under Appendix A at the end of this document.

4.6 Real Time Clock Support

For special applications requiring onboard date/time information a real time clock can be equipped.

4.7 Serial Line Interfaces

Along with the network interface, the Eth29-G also has two serial (RS232) ports S1 and S2.
The serial ports can be used as needed (e.g., for serial line IP, or for debug purposes). They are connected to the DUART I/O pins of the PowerQUICC II Pro.

4.8 USB Interfaces

The Eth29-G also has two USB 2.0 serial ports S3 and S4. They are master- and slave capable. If used as master, they may supply up to 500mA at +5V to each of the 2 interfaces. They connect to the USB I/O pins of the PowerQUICC II Pro through a USB3300 Dual PHY.
For further information please refer to the devices User's Manual, listed under Appendix A at the end of this document.

5 Eth29-G - Jumper Settings

The Eth29-G has been designed to adapt to a customers system by a minimum of hardware switches and jumpers. The location of the switches and jumpers is shown in section 4.1, "Eth29-G - Location Overview".

5.1 Setting the Board´s Base Address

The board´s VMEbus base address is set within the 32 bit address range using the hexadecimal rotary switches SW4-SW2. SW4 is used to set the 4 higher order bits (A31-A28) and SW2 sets the 4 lower bits (A23-A20). The default setting is:

Base address = $50C00000

In systems with a 24 bit address range, the base address is set using SW2 only.

Note: As the size of the onboard dual port memory is 4 MByte, the base address must always be aligned to a 4 MByte address boundary. So valid values for rotary switch SW2 are 0,4,8,C only.

5.2 Setting the VMEbus Interrupt Vector/Level

On the Ethe29-G the VMEbus interrupt vector and level is setable by software only. Any level (1 – 7) and any vector is programmable.

5.3 BDM Test Connector

The following table shows the pin out of the BDM connector. This connector is used for debugging and factory testing only.

Table 2: BDM Test Connector

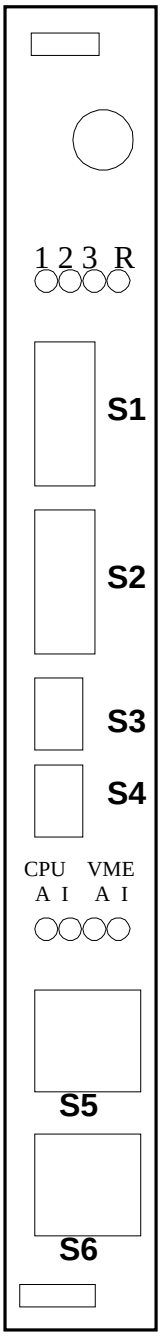
BDM Port				
	PIN			
TDO	1		2	nc
TDI	3		4	/TRST
nc	5		6	Vdd
TCK	7		8	CKSTP_IN
TMS	9		10	nc

/SRESET	11		12	nc
/HRESET	13		14	nc
CKSTP_OUT	15		16	GND

6 The Eth29-G Front-Panel

Mounted on the Eth29-G front panel are connectors for the serial and network interfaces, a reset switch, and a number of indicator LEDs. This chapter contains a detailed description of the various components mounted on the front panel.

Figure 2: The Eth29-G Front-Panel



Reset Pushbutton

Board Status Indicator LEDs
LED 1-3: programmable via CPU-Portpins
LED R: indicates RESET is asserted

RS232 Interfaces

USB Interfaces

Dualported RAM Access / IRQ LEDs
CPU A: indicates CPU access to SRAM
CPU I: indicates pending IRQ to CPU
VME A: indicates VME access to SRAM
VME I: indicates pending IRQ on VME

10/100/1000 BaseT Interface Connector RJ45 and Network Indicator LEDs
The connector integrated LEDs can be assigned several functions through CPLD registers and PHY-internal registers.

6.1 Reset Switch

This switch can be used to locally reset the Eth29-G board. After the reset, the board does a self-test and then initializes the basic firmware. A reset should never be made while the network is in operation, since this may have unpredictable consequences for the Master CPU.

6.2 Board Status Indicator LEDs

The board indicator LEDs are showing operational status for the onboard devices. The LEDs 1-3 are programmable by application software by configuring the CPU port pins listed in the table below.
The red LED labeled with 'R' is lighted when RESET is asserted.

Table 3: Programmable GP LEDs

LED	Color	CPU-Portpin
5	green	GPIO_ 1_4
6	green	GPIO_ 1_5
7	yellow	GPIO_ 1_6

6.3 Network Indicator LEDs

The network indicator LEDs are indicating the actual network line state. These LEDs are programmable by application software. Via registers implemented in the CPLD device, one LED per Ethernet channel can be controlled by the CPU in their color, and in its activity by the PHY's LED-outputs. The second LED per Ethernet channel is fully software programmable via CPU port pins like the table below shows.

Table 4: Programmable Network LEDs

LED	Color	CPU-Portpin
Eth1 A	Green/Red	GPIO_ 2_22
Eth1 K	Green/Red	GPIO_ 2_23
Eth2 A	Green/Red	GPIO_ 2_24
Eth2 K	Green/Red	GPIO_ 2_25

6.4 RS232 Interfaces - S1 and S2

The Eth29-G has two serial (RS232) interfaces which can be used at rates up to 38400 baud. The interfaces can be used as additional communications channels (e.g., for serial line IP or other serial communications protocols). The standard settings assign S1 as the output port for the firmware´s debugging and error messages.
Each serial interface uses a 9 pin Sub-D connector with the following pin assignment:

Table 5: RS232 Connectors

Pin	Assignment
1	NC
2	RXD
3	TXD
4	NC
5	GND
6	NC
7	RTS
8	CTS
9	NC

6.5 USB Connectors

- The Eth29-G has two USB interfaces which Support USB High Speed (480Mbit/s), Full Speed (12Mbit/s), and Low Speed (1.5 Mbit/s).

Each serial interface uses a 5 pin Mini-USB connector with the following pin assignment:

Table 6: USB Connectors

Pin	Assignment
1	VCC
2	D-
3	D+
4	ID
5	GND

6.6 10/100/1000 BaseT Connectors

This RJ45 is provided as the interface connector for 10BaseT to 1000BaseT network connection. Its pin-out is as follows:

Table 7: 10/100/1000 BaseT Connectors

Pin	Assignment
1	MDI0+
2	MDI0-
3	MDI1+
4	MDI1-
5	MDI2+
6	MDI2-
7	MDI3+
8	MDI3-

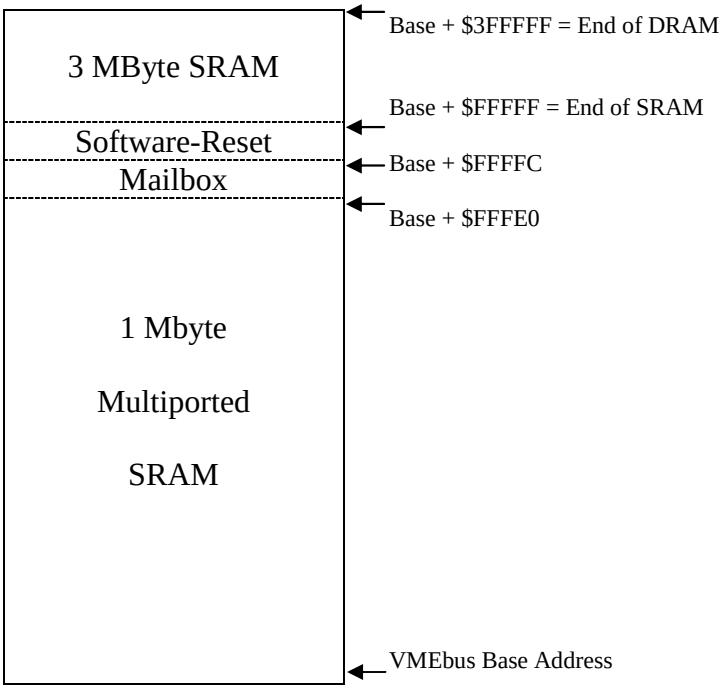
7 Address Ranges

This chapter presents the Eth29-G VMEbus and PowerQUICC II Pro memory maps.

7.1 VMEbus – Addresses

The Eth29-G occupies an address range of 1 or 4 MB on the VMEbus (factory setting). When accessed from the VMEbus these addresses are seen as a 1 or 4 MB bank of RAM (multiported communications SRAM/DRAM between the CPU and the VMEbus). This memory is equipped with 4 MByte fast SRAM.
The board's base address is set using the hexadecimal switches S1 - S3 (see section 3.1). When the board is used within a 24 bit VMEbus address range, switch S3 is used only.

Table 8: VMEbus – Addresses



The cells for the mailbox interrupt and the software-reset are located in the upper addresses.

7.2 PowerQUICC II Pro CPU - Memory Map

The CPU's memory map is shown below in figure 3. The dualported RAM at address 0xfa000000 is used for the communication between the VMEbus, and the local PowerQUICC II Pro CPU.

Table 9: PowerQUICC II Pro CPU - Memory Map

Address	**Device**
0xfc000000	Flash Memory
0xe0000000	I/O Devices
0xfa000000-0xfa3fffff	dualported RAM
0xfa0ffffc	Software Reset Cell
0xfa0fffe0	Mailbox Cell
0xfae00000	BIM
0xfae00100	FPGA Version Register
0xfaf00000	PowerQUICC internal Registers
0x0 – 0x07ffffff	CPU SDRAM - 128 MByte

7.3 PowerQUICC II Pro CPU - IRQ Map

The following table shows the assignment of the CPU's IRQ inputs to various on-board IRQ-sources.

Table 10: PowerQUICC II Pro CPU - IRQ Map

IRQ-Source	**CPU IRQ Input**
IRQ 3	SRAM-Bridge: IRQ from VME
IRQ 4	Ethernet PHY Ch.1 IRQ
IRQ 5	Ethernet PHY Ch.2 IRQ
IRQ 6	connected to COP-Header Pin 15
IRQ 7	connected to COP-Header Pin 8

8 Registers

8.1 Accessing Mailbox and Software-Reset Locations

A mailbox interrupt or a software reset can be triggered by writing to the appropriate memory cell. When read, these cells appear as normal RAM and it is thus possible to read which value was previously written to trigger the event.
Since the protocol firmware zeroes the mailbox interrupt cell after servicing the interrupt, it is possible to avoid triggering a new interrupt before the previous one has been handled. This characteristic allows the mailbox-cells to be used as semaphores between the Master board and the Slave board.
Both cells may be accessed as byte, word, or long-word.

8.2 FPGA internal Registers

8.2.1 FPGA Version Register

This 8-Bit Register holds the FPGA Version coded in two Nibbles, so that for example 0x13 would represent Version 1.3.

Table 11: FPGA Version Register

FPGA Version – Address Offset 0x0100								
Default value 0x10								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	FPGA Version Major				FPGA Version Minor			

8.3 CPLD internal Registers

8.3.1 PCB Version Register

This 8-Bit Register holds the PCB Version coded in two Nibbles, so that for example 0x13 would represent Version 1.3.

Table 12: PCB Version Register

PCB Version – Address Offset 0x0								
Default value 0x10								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	PCB Version Major				PCB Version Minor			

8.3.2 CPLD Version Register

This 8-Bit Register holds the CPLD Version coded in two Nibbles, so that for example 0x13 would represent Version 1.3.

Table 13: CPLD Version Register

CPLD Version – Address Offset 0x1								
Default value 0x10								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Func	CPLD Version Major				CPLD Version Minor			

8.3.3 CPLD Status/Control Register 1

This 8-Bit Register holds the status of the Broadcom Ethernet PHY LED / Interrupt I/Os as is at the time of reading. Also, the colour of the PHY-controlled LEDs in the RJ45 connectors can be selected.

Table 14: CPLD Status/Control Register 1

CPLD Version – Address Offset 0x2								
Default value 0xb								
Bit	7	6	5	4	3	2	1	0
Access	R/W	R	R	R	R	R	R	R
Reset Value	0	0	0	0	1	0	1	1
Func	LEDCOL	-	-	-	PHY pin LEDP2_2	PHY pin LEDP2_1	PHY pin LEDP1_2	PHY pin LEDP1_1

LEDCOL Colour of LED, 0 = green, 1 = red

PHY pin LEDP2_2 Status of PHY pin LEDP2_2
-
PHY pin LEDP1_1 Status of PHY pin LEDP1_1

8.3.4 CPLD Status/Control Register 2

This 8-Bit Register holds the status of the Broadcom Ethernet PHY LED / Interrupt I/Os as they were during last RESET when used as strapping pins, and the status of the set that can be used to reprogram them.

Table 15: CPLD Status/Control Register 1

CPLD Version – Address Offset 0x2								
Default value 0x0								
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Power-On Reset Value	0	0	0	0	0	0	0	0
Func	LEDP2_2_S	LEDP2_1_S	LEDP1_2_S	LEDP1_1_S	LEDP2_2_Reg	LEDP2_1_Reg	LEDP1_2_Reg	LEDP1_1_Reg

LEDP2_2_S Status of the PHY strapping pins during last RESET
-
LEDP1_1_S

LEDP2_2_Reg when this register is written for the 1st time after Power-On, the value of this bit field will be used to set up the PHY strapping pins during the
-
LEDP1_1_Reg next RESET (e.g. by writing the CPU RCR register).

8.3.5 CPLD Status/Control Register 3

This 8-Bit Register holds the status of miscellaneous strapping pins for CPU and FPGA. as they were during last RESET when used as strapping pins, and the status of the set that can be used to reprogram them.

Table 16: CPLD Status/Control Register 1

CPLD Version – Address Offset 0x2								
Default value 0x0								
Bit	7	6	5	4	3	2	1	0
Access	R	R/W	R/W	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Func	ConfDone	MSEL1	MSEL0	THERM0	LGPL5	LGPL3	LGPL1	LGPL0

ConfDone — 0 = FPGA configuration done

MSEL1 – 0 — MSELx strapping pins of the Altera Cyclone FPGA
For factory use only. Do not alter.

THERM0 — CPU strapping pin

LGPL5 – 0 — CPU strapping pins

9 Bus Interrupter Module

The Eth29-G board can trigger level 1-7 VMEbus vectored interrupts. The desired interrupt level can be set by software. The vector number is generally set by a user-modifiable program module (under OS-9, for example, the Device-Descriptor), which is passed to the firmware during initialization of the slave board and then written to the Bus Interrupter Module.

10 Known Bugs

none

Appendix A: Reference Documentation

[1] Freescale, MPC8349E PowerQUICC™ II Pro, Integrated Host Processor Family Reference Manual, Rev. 2, 12/2005
[2] Freescale, MPC8343E PowerQUICC™ II Pro, Integrated Host Processor Hardware Specifications, Rev. 6, 11/2005
[3] Freescale, MPC8347E PowerQUICC™ II Pro, Integrated Host Processor Hardware Specifications, Rev. 5, 10/2005
[4] Altera, Cyclone II Device Handbook, Volume 1, Cyclone II FPGA Family Data Sheet, V2.1, Nov. 2005
[5] Broadcom, BCM5482 Data Sheet, 10/100/1000BASE-T Gigabit Ethernet Transceiver, 5/2005
[6] Samsung, DDR SDRAM 256Mb F-die (x16), 256Mb F-die DDR SDRAM Specification, Rev. 1.3, July 2005
[7] Alliance Semiconductor, AS9C25256M2036L, AS9C25128M2036L, 2.5V 256/128K X 36 Synchronous Dual-port SRAM with 3.3V or 2.5V interface, V1.3, 9/2004
[8] SMSC, USB3300 Hi-Speed USB Host, Device or OTG PHY with ULPI low pin interface, Datasheet, Rev. 1.03, 5/2005

Appendix B: Document's History

Version	Date	Description	Author
1.0	26.01.2006	Initial Version	ga
1.1	25.10.2006	Adapted to HW Rev. 1.1	ga
1.2	06.06.2007	chapters 1.2. added	ga
1.3	13.10.2008	Changed chapter ordering and added Board specification chapter	ks
1.4	09.01.2009	Fixed mismatch in VME address switch documentation	te
1.5	23.01.2009	Added note about VMEbus address alignment	hl